Remarks

Claims 13-15, 30-32 and 38-40 were rejected as being anticipated by Kohno et al. (U.S. Patent No. 6,523,125). Claims 1-2, 5-12, 16-17, 20-27, 29 and 34-37 were rejected as being unpatentable over Matsushima et al. (U.S. Patent No. 5,875,120) in view of Thomas (U.S. Patent No. 6,601,181). Claims 3-4 and 18-19 were rejected as being unpatentable over Matsushima in view of Thomas, and in further view of Mustafa et al.(U.S. Patent No. 6,243,831). Claim 28 was rejected as being unpatentable over Matsushima 16 in view of Thomas as applied to claim, and in further view of Sadashivaiah (U.S. Patent No. 5,638,541). Claim 33 was rejected as being unpatentable over Kohno in view of Sadashivaiah. Claims 16, 32, 34 and 38 were objected due to informalities.

In response, Applicants have amended cancelled claims 14, 31 and 39, and amended claims 13, 16, 30, 32, 34 and 38. Applicants respectfully request reconsiderations for at least the reasons set forth.

Claim Objections

Claims 16, 32, 34 and 38 have been amended to overcome the informalities objections, and not for overcoming any prior art. No new matter has been introduced.

Claim Rejections under 35 USC § 102(e)

It is well settled that 102 rejection requires clear anticipation from the prior art. While both the method of claim 13 and the method of Kohno are designed to power up a system at a saved operational state, the method of claim 13 and the method of Kohno are very different, and neither anticipate the other.

The method of claim 13 specifically requires that as part of a cold start reset process, a BIOS is employed to determine whether a valid saved operational state

exists. Further, also as part of the cold start reset process, the BIOS, on determination of the existance of a valid saved operational state, is employed to invalidate the valid saved operational state, and to transfer the saved operational state into memory. Then, on completion of the transfer, the BIOS is to invoke a "resume" process through a wake event to continue the start up process.

Note that the "invalidation" is directed against the saved operational state, and the transfer of the saved operational state is performed prior to the invocation of the resume process through a wake event.

In contrast, Kohno teaches as part of the start up process from the un-powered state, determining whether the system is in a hiberation mode, by examining whether there is a valid hiberation signature. Even if we assume the determination of the existence of a valid hiberation signature can be read as having effectively anticipated the recited determination of the existence of a valid saved operational state (which Applicants disagree but need not address at the present time), the invalidation of the hiberation signature does not anticipate invalidation of the saved operational state. The term "hiberation signature" refers to "information indicating that the system is in the hiberation mode" (see Kohno col. 4, lines 8-9). A saved operational state does not necessarily indicate the system is in a hybernation mode. Thus, the invalidation of the hiberation signature under Kohno, when the configuration of the system has changed, does not anticipate the required invalidation of a valid saved operational state.

Further, under Kohno, the transfer of the saved operational state is after "wake up", not before "wake up" as required by claim 13. See e.g. Kohon, col. 19, lines 33-35 where it is stated "… if the hibernation signature is set, it is meant that power up at step S200 is a wake up rather than POR …", which precedes "restoration of data", operational S210.

Thus, for at least the foregoing reasons, Kohno fails to anticipate at least one recited element of claim 13. Accordingly, claim 13 is patentable over Kohno under 35 USC 102(e).

Rejection of claim 14 has been reendered moot by its cancellation.

Claim 15 depends and adds from claim 13; therefore for at least the same reasons claim 13 is patentable over Kohno, claim 15 is patentable over Kohno.

Regarding claim 30 and claim 38, each includes in substance the distinguishing recitations discussed above for claim 13. Thus, for at least the same reasons claim 13 is patentable over Kohno, claims 30 and 38 are also patentable over Kohno.

Rejections against claims 31 and 39 have been renedered moot by their cancellations.

Claims 32 and 40 depend from claims 30 and 38, incorporating their recitations resepectively; thus for at least the same reasons claims 30 and 38 are patentable over Kohno, claims 32 and 40 are patentable over Kohno.

Claim Rejections under 35 USC § 103(a)

Section 103 explicitly requires an invention be viewed as a whole. When so viewed, claim 1 is directed towards a method of saving the operational state of a system by having a BIOS intervenes in a suspend process initiated in response to an AC failure. During the intervention, in addition to initiating a number of data transfer operations to save the operational state, the BIOS is further to check periodically whether data transfer operations are completed, and in bewteen the checking, cause the processor to operate in a reduced power conumption state.

Matsushita's teachings relied by the Examiner, merely speaks in generality of a suspend mode, where the power supply to all circuits are halted, except for the main memory, after the data required for resuming the task are saved in the main memory (column 2, lines 1-8), of checking whether data transfer operations are completed (col 5, lines 46-47), and of halting the CPU during the time period required for reading and writing to the disk (col. 7 lines 58-62).

Matsushita does not teach or suggest having these operations performed by the BIOS, let alone having these operations performed by the BIOS as part of an intervention into a suspend process. Further, Matsushita's teaching of halting the CPU is for the time required for reading and writing to the disk, which is tied to the time for performing data transfer, thus does not suggest the recited operating of the CPU in a power reduced mode in between checking for data transfer completion, which is not tied to the time for performing data transfer to a disk.

Thomas is cited for his teachings of saving the system's state to memory when AC power is removed. Thus, even combining Matsushita with Thomas, the combination still does not suggest the required intervention of a suspend operation using a BIOS, nor having the BIOS cause the processor to operate in a power reduction mode in between checking for data transfer completion during the intervention.

Applicants submit but for impermissible application of hindsight, applying Applicants teachings, one of ordinary skill in the art would not arrive at the claimed invention based on the combined teachings of Matsushita and Thomas. Therefore, claim 1 is patentable over Matsushita and Thomas, under 35 USC 103(a).

Claims 2, 5-12 add and depend on claim 1 with all its recitation; thus, for at least the same reasons claim 1 is patentable over Matsushita in view of Thomas, claims 2, 5-12 are also patentable over Matsushima in view of Thomas.

Claims 16 and 34 includes in substance the distinguishing recitations discussed above for claim 1. Thus, for at least the same reasons, claims 16 and 34 are patentable over Matsushima and in view of Thomas.

Claims 17, 20-27, 29 add and depend on claim 16 with all its recitation; thus, for at least the same reasons claim 16 is patentable over Matsushita in view of Thomas, claims 17, 20-27, 29 are also patentable over Matsushima in view of Thomas.

Claims 35-37 add and depend on claim 34 with all its recitation; thus, for at least the same reasons claim 34 is patentable over Matsushita in view of Thomas, claims 35-37 are also patentable over Matsushima in view of Thomas.

Claims 3-4 and 18-19 were rejected as being unpatentable over Matsushima in view of Thomas, and in further view of Mustafa. Claim 2 adds and depends on claim 1, and claim 3 further adds and depends on claim 2. Regarding claim 1, the teaching of Mustafa does not cure the previously discussed deficiencies of the combination of Matsushima and Thomas, therefore claim 1 remains patentable over Matsushima and in view of Thomas, and in further view of Mustafa. For at least the same reasons, claims 3-4, 18-19 that add and depend on claim 1 and claim 2 with all its recitations are patenable over Matsushima,

Even if we disregard the deficiencies of Matsushima and Thomas, Mustafa merely teaches of a microprocessor exhibiting a reduced power states in response to a predetermined conditions such as: a user pressing a standby button, or an expiration of a time period (column 9, lines 14-15, and lines 26-3. Mustafa fails to instructs of the method of claim 1, where at least a processor to operate in a reduced power mode in at least one time period while the BIOS is not performing said checking (whether the data transfer is completed). Mustafa also speaks of BIOS saving RAM to a hibernation file (column 6, lines 36-39), and it does not occur in ACPI-defined S1, S2, S3, or S4 states (column 6, lines 40-48); Mustafa still fails to teach of the BIOS checking if the data

transfer is completed, and the BIOS causing a processor to enter an ACPI C1 state for the first time period while the BIOS is not performing the said checking (as cited in claim 3). Therefore, claim 3 that depends and adds to claim 2 (that adds and depend on claim 1) remains patentable over Matsushima in view of Thomas, even in further view of Mustafa.

Claims 3-4, and 18-19 add and depend on claim 1 and claim 2 with all their recitations; thus, for at least the same reasons claim 1 is patentable over Matsushima and in view of Thomas, and in further view of Mustafa, claims 3-4 and 18-19 are also patentable over Matsushima and in view of Thomas, and in further view of Mustafa.

Regarding claim 28, it was rejected as being unpatentable over Matsushima in view of Thomas as applied to claim 16, and in further view of Sadashivaiah. As previously discussed, Matsushima in view of Thomas fails to disclose the system of claim 1. Claim 16 includes in substance the distinguishing recitations discussed above for claim 1. For at least the same reasons claim 1 is patentable over Matsushima in view of Thomas, claim 16 is also patentable over Matsushima and in view of Thomas. The teaching of Sadashivaiah does not cure the previously discussed deficiencies of the combination of Matsushima and Thomas as applied to claim 16; therefore, for at least the same reasons claim 16 is patentable over Matsushima in view of Thomas, claim 16 remains patentable over Matsushima in view of Thomas, and in further view of Sadashivaiah. Claim 28 adds and depends on claim 16 with all its recitation; thus, for at least the same reasons claim 16 is patentable over Matsushima in view of Thomas and in further view of Sadashivaiah, claim 28 remains patentable over Matsushima in view of Thomas and in further view of Sadashivaiah.

Claim 33 was rejected as being unpatentable over Kohno in view of Sadashivaiah. Claim 33 adds and depends on claim 30 with all its recitation; thus for at least the same reasons claim 30 is patentable over Kohno, claim 33 is also patentable over Kohno. The teachings of Sadashivaiah does not alleviate the

discrepancies of Kohno; thus, for at least the same reasons claim 33 remains patentable over Kohno, claim 33 still remains patentable over Kohno and in view of Sadashivaiah.

Conclusion

In conclusion, claims 1-13, 15-30, 32-38 and 40 are in condition for allowance. Early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 09/05/2006

/Al AuYeung/
Al AuYeung
Registration No. 35,432

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981